SRIRAM VENKATESH

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OBJECTIVE: Seeking full-time opportunity for a Physical Design/CAD/Methodology Engineer position

EDUCATION

UNIVERSITY OF CALIFORNIA, SAN DIEGO — **SAN DIEGO, CA**
M.S. in Computer Engineering, CSE Department, GPA: 3.825/4 — *Sep 2016 - Present*

BITS-PILANI — **PILANI, INDIA**
B.E. in Electrical and Electronics Engineering, GPA: 8.20/10 — *Aug 2009 – Jun 2013*

EMPLOYMENT

APPLE — **AUSTIN, TEXAS**
Summer Intern, 3 months — *Jun 2017 – Sep 2017*

- Worked on techniques for power reduction in the Synthesis, Place and Route (SP&R) flow - for the graphics processor at advanced technology nodes

ARM HOLDINGS — **BANGALORE, INDIA**
Physical Design Engineer, 3 years — *Jul 2013 – Jun 2016*

- **Project 1:** Performed SP&R of ARM Mali v550 Video Processor Core and Cluster on 16FinFet+ technology node, using Cadence Genus and Innovus; handled STA and DRC using Synopsys PrimeTime and Mentor Calibre
  Implemented multi-domain 1801 power intent; performed Static and Dynamic power analyses using Ansys Redhawk
- **Project 2:** Worked on the benchmarking of ARM Generic Interrupt Controller on 28 HPM technology, by doing Place & Route trials and providing RTL feedback and frequency benchmarks

Presented a paper and a poster on "Alternate Power Grid Pattern for lower IR drop" at ARM-Cambridge and Bangalore.

LSI INTEGRATED — **PUNE, INDIA**
Intern, 6 months — *Jan 2013 – Jun 2013*

- Physical Design and Static Timing Analysis of 2 blocks of a network processor on 28nm technology node.

RESEARCH EXPERIENCE

VLSI CAD LABORATORY — **UCSD, SAN DIEGO**
Graduate Student Researcher — Sep *2016 – Present*
Advisor: Prof. Andrew B. Kahng. Working on CAD improvements for **Routing** and **CTS** design methodologies

- **Project 1:** Algorithm for improved routing trees for high performance chips (With Cadence)
- **Project 2:** Improved clock routing strategy for better model-hardware correlation (with Samsung)

COURSES AND CERTIFICATIONS

- Graduate Coursework
  - VLSI Digital Systems Algorithms & Architecture, Principles of Computer Architecture, Embedded Systems
- Undergraduate Coursework
  - Analog & Digital VLSI Design, Digital Electronics & Computer Organization
- **ARM Accredited Engineer** (2015) - received certification for ARM v7 architecture.

ADDITIONAL EXPERIENCE AND AWARDS

- Served as a Teaching Assistant for the course 'Circuits and Signals' at BITS-Pilani
- Coordinated a group of 25 students to conduct events during inter-university sports, cultural and technical festivals of BITS-Pilani
- Bagged 3rd prize for the project 'Electromagnetic Surveillance Weapon' during the 2011 Tech-Fest of BITS-Pilani
- Organized and hosted events at the ARM Bangalore office as part of the ARM Fun-During-Work team – which helped in increasing employee productivity and satisfaction

SKILLS

- EDA Tools — Cadence Genus, Innovus, Conformal Low Power, Voltus, Virtuoso
  Synopsys PrimeTime, ICC; Ansys Redhawk; Mentor Calibre
- Languages — C, C++, Tcl, Python
  Verilog, ARM Assembly